#5/Election/A
10/29/02
Mollis L

I hereby certify that this correspondence is being sent on this date by Facsimile to The Commissioner of Patents & Trademarks, Washington, D.C. 20231 to Facsimile Transmission Number 703-872-9318

25 October 2002
Date of Deposit

Graham S. Jones, II, Reg. No. 20,429
Name of Person Making Deposit

Signature

25 October 2002
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Brofman et al.	Date:	25 October 2001
Application No.	09/870,531	Examiner:	James M. Mitchell
Filing Date:	31 May 2001	Art Unit:	2827
Title:	Method of Manufacture of Silicon Based Package and Device Manufactured Thereby	Attorney:	Graham S. Jones, II 42 Barnard Avenue Poughkeepsie, NY 12601-5023

RESPONSE TO REQUIREMENT FOR RESTRICTION

Assistant Commissioner for Patents
Washington, D. C. 20231

Your Honor:

In response to the Office Action of 27 August 2002, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

A1

1. (Amended) A method comprising:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for a silicon based package (SBP),

forming an interconnection structure including multilayer conductor patterns over the first surface,

forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure,

thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,

forming via holes which extend through the UTSW, and

forming metallization in the via holes with the metallization extending through the UTSW.

Serial No.:	09/ 870,531	Art Unit:	2827

A2

14. (Amended) A method comprising:

providing a base for a silicon based package (SBP) comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

15. (Amended) The method of claim 14 including the steps as follows:

forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

followed by planarizing the via/cap pad layer down to the surface of the dielectric layer, thereby forming the metal vias in the via holes.